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# Series-Tuned High Efficiency RF-Power Amplifiers

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**Abstract**—An approach to high efficiency RF-power amplifier design is presented. It addresses simultaneously efficiency optimization and peak voltage limitations when transistors are pushed towards their power limits.

## I. INTRODUCTION

A major decision in design of a high efficiency RF-power amplifier stage is to determine the transistor load impedance, which simultaneously provides the desired output power, optimizes efficiency, and operates the transistor within its voltage ratings. Having solved this problem, the remaining task is to design the corresponding impedance transformation and matching circuits for the transistor. Here, we may benefit from the still improving accuracy of the simulation models of RF power transistors. It is the purpose of this paper to focus on the first issue, and subsequently demonstrate how the results may support a 50W, 435MHz narrow-band RF power amplifier design using vendor supplied transistor models.

## II. SERIES TUNING IN RF POWER AMPLIFIERS

High powers at high frequencies imply low impedance levels, and series tuning becomes the natural choice of connecting to the transistor through realizable component. Series tuning means also that the currents entering the transistor are kept sinusoidal. This is in contrast to the classical class A, AB, B, and C RF-power amplifier concepts, where parallel tuning forces sinusoidal voltages. Series tuning is the outset for more dedicated high efficiency amplifier principles including class D, F, and, especially, class E. Therefore, the basic equivalent circuit setup for discussing series tuning, which is shown in Fig.1, resembles the setups for class E discussions. But unlike the common approach in literature, [2] [3], no attempts are made to find closed or partly closed form solutions to this circuit problem. Instead we shall resort on numerical techniques and demonstrate that the corresponding solutions have wider practical implications since only a minimum number of constraints are required. Furthermore, it becomes possible to incorporate transistor series losses in the efficiency estimations, which significantly improves the foundation for design decisions.

In addition to the series tuning, which causes the sinusoidal load current of amplitude  $I_{d1}$ , the major assumptions behind

the equivalent circuit is that the transistor is driven so hard that its operation may be described by a switch. The switch is closed when the gate to source voltage is above threshold and open when it is below. The transistor input details are not explicitly shown in the equivalent circuit, but the input driving is specified through the switch opening angle  $\theta_a$ . When the switch is open, the total drain current, which is the sinusoidal load current plus the dc supply current  $I_{d0}$ , charges or de-charges the transistor output capacitance  $C_o$ . When the switch closes and short-circuits the capacitor, the drain source voltage is fixed to the voltage source  $V_{ON}$ , which accounts for the dynamic on-voltage of the transistor.

Before discussing the setup and solution of equations for the output loading, it should be realized that the circuit includes two power loss mechanisms. The transistor series loss,

$$P_{tr,series} = I_{c0} V_{ON} , \quad (1)$$

and the switching loss that accompanies the closing of the switch. If  $V_{csw}$  denotes the capacitor voltage prior to switching,  $f_0$  is the operating frequency, and  $B_c$  is the corresponding susceptance of the output capacitor, the switching loss becomes

$$P_{tr,switch} = C_o V_{csw}^2 f_0 / 2 = B_c V_{csw}^2 / 4\pi , \quad (2)$$

The power balance in the circuit is given by

$$\begin{aligned} P_{load} &= P_{battery} - P_{tr,series} - P_{tr,switch} \\ &= I_{d0} V_{DD} - I_{d0} V_{ON} - P_{tr,switch} , \end{aligned} \quad (3)$$

where  $V_{DD}$  is the supply voltage. If we organize the circuit to avoid switching losses, which is a part of the class E concept, the drain efficiency becomes the highest possible,

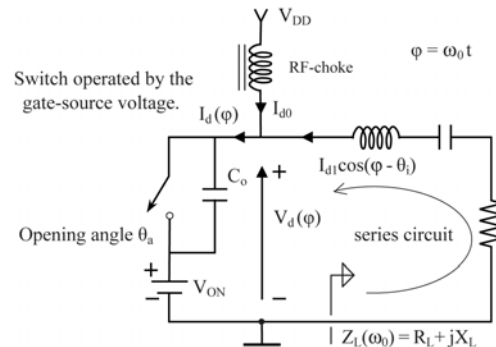


Figure 1. Simplified equivalent circuit for transistor loading in a series tuned amplifier.

This work was conducted as the initial step towards the design of a power amplifier for a p-band ice sounding radar, ESA (European Space Agency) contract no 19397/05/NL/JA. [1]

$$\eta_{opt} = P_{load} / P_{battery} \Big|_{P_{r,switch}=0} = 1 - V_{ON} / V_{DD} . \quad (4)$$

Without series losses either, this result agrees with the ideal class E promise of 100% efficiency. In realistic amplifiers the efficiency in (4) represents an upper bound for any design.

### III. MODEL SETUP

Fig.2 summarizes the assumed wave-shapes of the drain current,

$$I_d(t) = I_{d0} + I_{d1} \cos(\varphi - \theta_i) , \quad \varphi = \omega_0 t, \quad (5)$$

and the drain voltage,

$$V_d(\varphi) = \begin{cases} V_{ON} + \frac{1}{B_c} \int_0^\varphi I_d(\varphi) d\varphi & 0 < \varphi < \theta_a \\ = \frac{I_{d0}}{B_c} \varphi + \frac{I_{d1}}{B_c} [\sin(\varphi - \theta_i) + \sin \theta_i], & \theta_a < \varphi < 2\pi. \end{cases} \quad (6)$$

The instance where the switch opens is taken as time origin above, so the switch open period of length  $\theta_a$  starts from zero. Within this period, the voltage gets an optimum if and when the current turns negative at phase  $\theta_m$ . We shall avoid lengthy discussions of pathological cases, and assume that this happens as sketched in Figure 2. , so the voltage peaks at phase

$$\theta_m = \theta_i + \pi - \cos^{-1}(I_{d0} / I_{d1}) . \quad (7)$$

The voltage expression (6) provides a basis for formulating three basic constraints that always must be met. First, the mean voltage must equal the battery voltage<sup>1</sup>,

$$\frac{1}{2\pi} \int_0^{2\pi} V_d(\varphi) d\varphi = V_{d0}(I_{d0}, I_{d1}, \theta_i, \theta_a, B_c, V_{ON}) = V_{DD} . \quad (8)$$

Taking the fundamental frequency drain voltage and current components as phasors, the loading condition is expressed

$$\vec{V}_{d1} = -Z_L \vec{I}_{d1} = -(R_L + jX_L) \vec{I}_{d1} , \quad (9)$$

where  $R_L$  and  $X_L$  are the real and the imaginary part of the load impedance. Worked out in details, this gives two loading constraints for in-phase and quadrature components respectively,

$$\begin{aligned} \frac{1}{\pi} \int_0^{2\pi} V_d(\varphi) \cos \varphi d\varphi &= V_{d1I}(I_{d0}, I_{d1}, \theta_i, \theta_a, B_c) \\ &= -I_{d1} [R_L \cos \theta_i + X_L \sin \theta_i] , \end{aligned} \quad (10)$$

$$\begin{aligned} \frac{1}{\pi} \int_0^{2\pi} V_d(\varphi) \sin \varphi d\varphi &= V_{d1Q}(I_{d0}, I_{d1}, \theta_i, \theta_a, B_c) \\ &= -I_{d1} [R_L \sin \theta_i - X_L \cos \theta_i] \end{aligned} \quad (11)$$

<sup>1</sup> Expression details are summarized below in the appendix

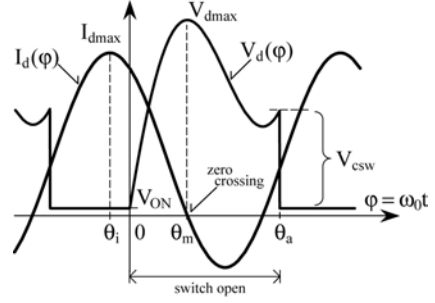


Figure 2. Drain current and voltage waveshapes in the switching equivalent circuit of Figure 1.

By equations (8), (10), and (11) we have established three relations among a set of nine variables and parameters

$$\{I_{d0}, I_{d1}, \theta_i, \theta_a, R_L, X_L, B_c, V_{ON}, V_{DD}\} . \quad (12)$$

Clearly, some of the components are fixed constants in a design task, but still more constraints are required to solve the transistor loading problem. Relevant candidates are

$$\text{Output Power : } P_{out} = R_L I_{d1}^2 / 2 , \quad (13)$$

$$\text{Efficiency : } \eta = R_L I_{d1}^2 / 2 I_{d0} V_{DD} , \quad (14)$$

$$\text{Maximum Current : } I_{dmax} = I_{d0} + I_{d1} , \quad (15)$$

$$\text{Maximum Voltage : } V_{dmax} = V_d(\theta_m) , \quad (16)$$

$$\text{No Switching Loss : } V_{csw} = V_d(\theta_a) - V_{ON} = 0 . \quad (17)$$

The last condition is a prerequisite for class E operation, but in literature, it is commonly followed by the additional requirement that the current through the switch must be zero at the switching instant. This condition is referred to as "optimal" switching, although it is hard to follow the rationale behind the term as the condition, which reads,

$$\begin{aligned} \text{"Optimal" Switching :} \\ I_d(\theta_a) = I_{d0} + I_{d1} \cos(\theta_a - \theta_i) = 0 , \end{aligned} \quad (18)$$

does not influence the efficiency of the amplifier. There are, however, two implications of (18). The nice property is that it becomes a remedy in setting up closed form design equations for class E amplifiers. The bad property is that it unnecessarily worsens the well known draw-back of class E designs, [3] p.170, namely that the maximum drain voltage approaches or exceeds the transistor voltage ratings, if we tend to operate them towards their maximum power capabilities. Since the strategy in the present work is to solve the design equations numerically, there are no needs for considering the condition in (18) here.

### IV. NUMERICAL SOLUTION

To demonstrate a numerical solution to the amplifier loading problem, we consider the task of designing a 50W, 435MHz, narrowband amplifier using the MRF373A LDMOS transistor from Freescale with 28V supply voltage. The transistor may be used to 75W and it has a drain voltage rating of

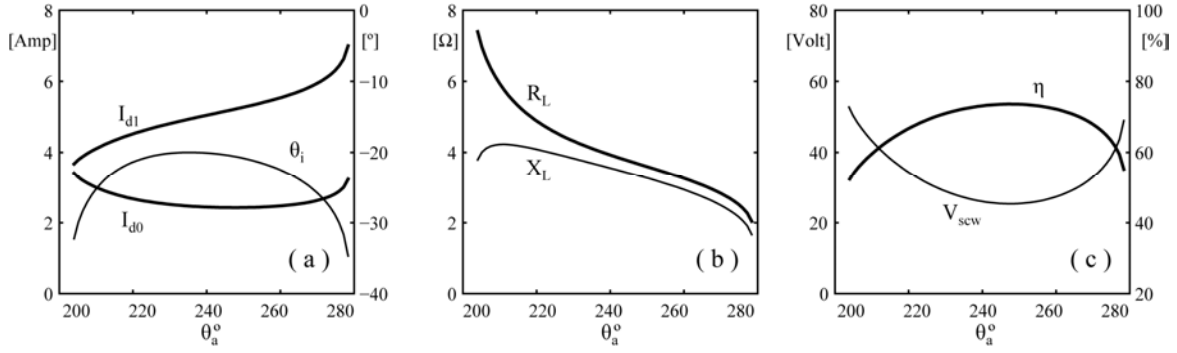


Figure 3. Part (a) and (b) hold the numerical solutions to the loading problem (8), (10), (11) subject to output power (13) and maximum voltage (16) constraints. The amplifier efficiencies and switched voltages in part (c) are post-calculated by (14) and the first equation in (17).

70V. To stay safe we shall limit the maximum drain voltage to 80% of the rating. The transistor has an output capacitance of 49pF and the dynamic on-voltage is set to 4.5V. Thereby three of the quantities in (11) are initially fixed,

$$B_c = 0.134 S, \quad V_{ON} = 4.5V, \quad V_{DD} = 28V. \quad (19)$$

In the solution process, the switch opening angle  $\theta_a$  is swept as an independent variable, and the numerical process must solve for the remaining five unknowns,  $I_{d0}$ ,  $I_{d1}$ ,  $\theta_i$ ,  $R_L$ , and  $X_L$ . Besides the three basic conditions (8), (10), and (11), the output power (13) and the maximum voltage (16) requirements are enforced using

$$P_{out} = 50W, \quad V_{d,max} = 56V. \quad (20)$$

The actual solution process is undertaken by the “fsolve” equation solver routine from the optimization toolbox in MATLAB, and we get the results that are shown in Fig.3. The horizontal axes span the whole range of opening angles  $\theta_a$  where the solutions are meaningful, real-valued quantities. The unknowns that are determined by the numerical process are shown in Fig.3 (a) and (b). On basis of the solutions the resultant efficiency and the voltages  $V_{scw}$ , which are short-circuited by the switch, are calculated and shown in Fig.3(c).

It is obvious that there is a simultaneous maximum in efficiency and minimum in  $V_{scw}$ . For a series-tuned amplifier with

maximum efficiency, the solution curves provide the following design data,

$$\theta_a|_{\max, \eta} = 247^\circ \Rightarrow \eta = 73.6\%, \quad R_L = 3.70\Omega, \quad X_L = 3.35\Omega. \quad (21)$$

The result shows that the penalty for staying with a safe maximum drain voltage is a reduction in efficiency from the upper bound in (4), which gives,

$$\eta_{opt} = 1 - 4.5/28 = 0.84 \quad \square \quad 84\%. \quad (22)$$

## V. AMPLIFIER DESIGN SUMMARY

The schematic of the final amplifier is shown in Fig.4 by the corresponding simulation setup for ADS (Advanced Design System from Agilent). The transistor model to be employed comes from the design library that may be downloaded from Freescale. Series tuning is enforced in the circuit by series connecting inductors in the signal path directly to the transistor terminals leads (short, broad transmission lines). At the output side of the transistor  $L_{o1}$ ,  $C_{o1}$ , and  $C_{o2}$  transform the external load to the drain load impedance in (21). Before the input matching circuit was established, the correctly loaded circuit was driven by a sinusoidal current, which was adjusted to provide the desired output power in simulation. By this step we implicitly incorporate the opening angle in the practical

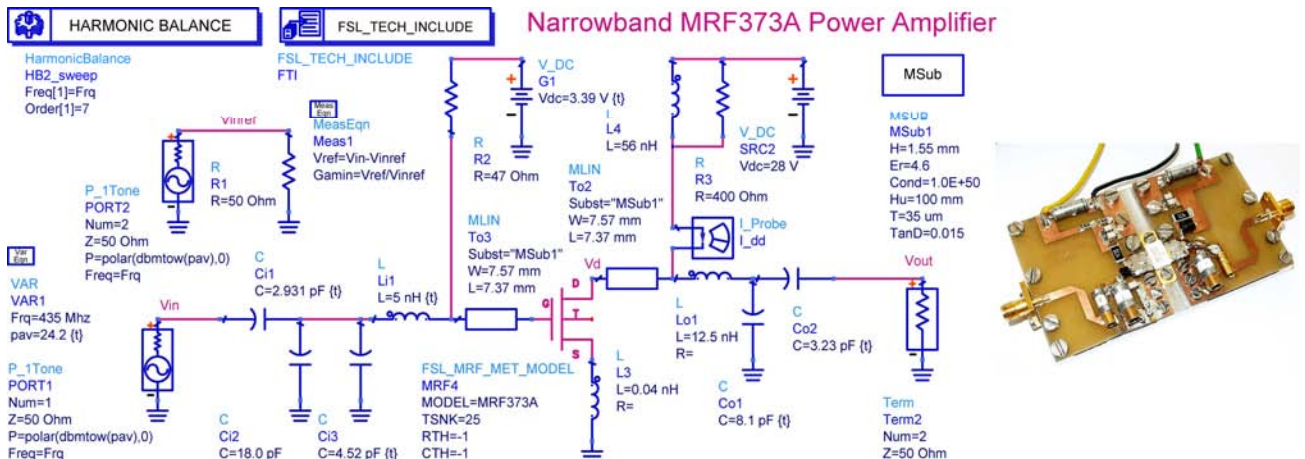


Figure 4. ADS simulation setup for a narrowband power amplifier that is loaded for maximum efficiency according to (21). Inset shows actual circuit.

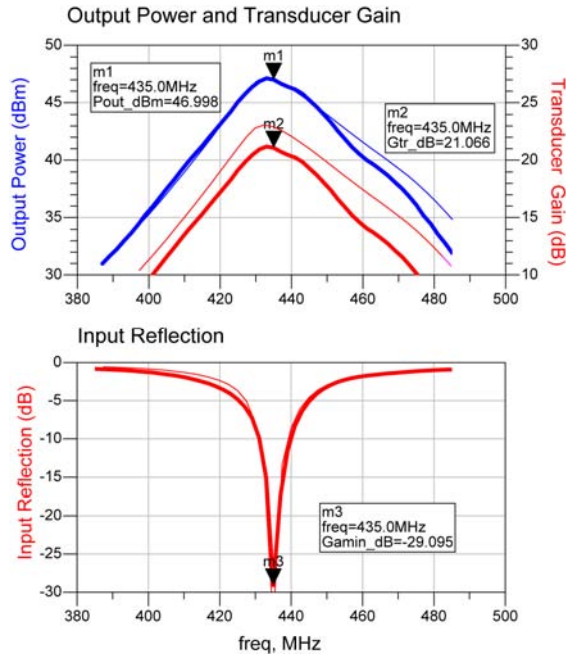


Figure 5. Measured (heavy lines) and simulated (thin lines) frequency responses of the circuits in Fig.4.

design process. It is done by recording and, subsequently, by power matching to the corresponding large signal input impedance through the  $L_{i1}$ ,  $C_{i1}$ , and  $C_{i2}$  circuit.

The frequency characteristics for output power, gain, and input matching achieved by this approach are summarized by Fig.5 and Table I.

TABLE I. AMPLIFIER PERFORMANCE

	$P_{out}$ [W]	Eff. %	$I_{DD}$ [A]
Measured	50.1	68.0	2.63
Simulated (ADS)	50.1	78.0	2.30
Switch Model	50.0	73.6	2.43

## VI. DISCUSSIONS AND CONCLUSIONS

Considering the three levels of methods and result that are summarized by Fig.5 and TABLE 1, they are in remarkably good agreement compared to RF power amplifiers simulation standards, so the series tuning approach, which was presented in this paper, has proven useful in practice.

There is room for improvement in the series tuned switch model of the transistor loading. This becomes clear, if we consider the wave-shapes of the simulated drain voltages and currents in Fig.6. It is seen that the assumption of a constant dynamic on-voltage is reasonable. The switching in the simulation, however, is not instant and the dynamic on-voltage is not completely constant. It should be investigated how we may compensate for a finite switching period and make a more refined on-voltage description, like it was done in an earlier

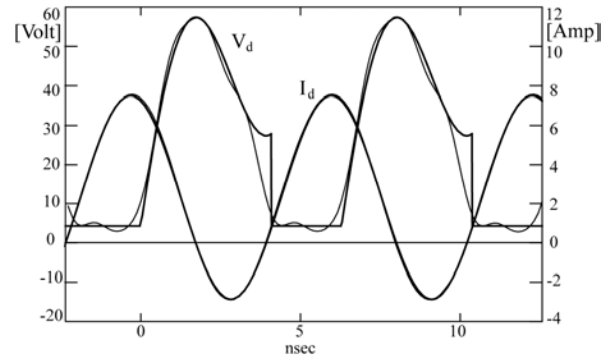


Figure 6. Simulated current and voltage wave-shapes (thin lines) compared with the similar switch model wave-shapes (heavy lines). The sinusoidal currents can hardly be distinguished.

successful attempt to cope with bipolar power-amplifiers in a similar way [4].

Regarding simulations, where the supplied model seems to overestimate realities, it should be kept in mind that the prevailing situation a few years ago was that practically no RF power amplifier designer trusted any form of simulations. It is demonstrated above that the quality of the simulation models have reached a level where they successfully may contribute to the design process, here by translating simplified theoretical design criteria into useful circuit matching parameters.

## APPENDIX, VOLTAGE COMPONENTS IN (8),(10), AND (11)

$$V_{d0}(I_{d0}, I_{d1}, \theta_i, \theta_a, B_c, V_{ON}) = V_{ON} + \frac{1}{2\pi B_c} \left[ \frac{I_{d0}^2 \theta_a^2}{2} + I_{d1} \{ \theta_a \sin \theta_i + \cos \theta_i - \cos(\theta_a - \theta_i) \} \right] \quad (23)$$

$$V_{d1l}(I_{d0}, I_{d1}, \theta_i, \theta_a, B_c) = \frac{1}{\pi B_c} \left[ I_{d0} (\cos \theta_a + \theta_a \sin \theta_a - 1) + \frac{I_{d1}}{4} \times \{ -2\theta_a \sin \theta_a - \cos(2\theta_a - \theta_i) + \cos \theta_i + 4 \sin \theta_i \sin \theta_a \} \right] \quad (24)$$

$$V_{d1Q}(I_{d0}, I_{d1}, \theta_i, \theta_a, B_c) = \frac{1}{\pi B_c} \left[ I_{d0} (\sin \theta_a - \theta_a \cos \theta_a) + \frac{I_{d1}}{4} \times \{ 2\theta_a \cos \theta_a - \sin(2\theta_a - \theta_i) + 3 \sin \theta_i - 4 \sin \theta_i \cos \theta_a \} \right] \quad (25)$$

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